IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of	:	
Jeong-Hwan Yang	:	Group Art Unit: 2812
Serial No.: 10/801,651	:	Examiner: Walter L. Lindsay Jr.
Filed: March 17, 2004	:	

SEMICONDUCTOR DEVICE WITH DIFFERENT LATTICE PROPERTIES

DECLARATION UNDER 37 C.F.R. ¶1.131

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I, Jeong-Hwan Yang, hereby declare as follows:

1. that I am an employee of Samsung Electronics Co., Ltd. (SEC), located in the Republic of Korea, and that the activities described in paragraphs 2 – 5 of this Declaration took place in the Republic of Korea and during my employment with SEC;

2. that I am the sole-inventor of the subject matter defined by the claims of the above-identified application;

3. that on or prior to October 21, 2002, I invented the subject matter defined by the claims of the above-identified application;

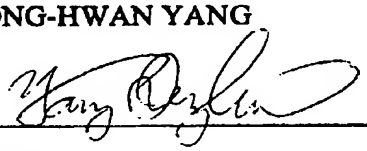
4. that on or prior to October 24, 2002, I prepared or caused to be prepared the attached "DISCLOSURE OF EMPOLYEE'S INVENTION";

5. that on or prior to October 24, 2002, I submitted or caused to be submitted the aforementioned "DISCLOSURE OF EMPLOYEE'S INVENTION" to the patent department of SEC's semiconductor division.

The undersigned being warned that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements and the like may jeopardize the validity of the application or document or any patent resulting there from, further declares that all statements made of his/her own knowledge are true; and all statements made on information and believe are believed to be true.

Respectfully submitted:

JEONG-HWAN YANG



Signature

03/28/2006

Date

Attachment: DISCLOSURE OF EMPOLYEE'S INVENTION

본 양식의 특징

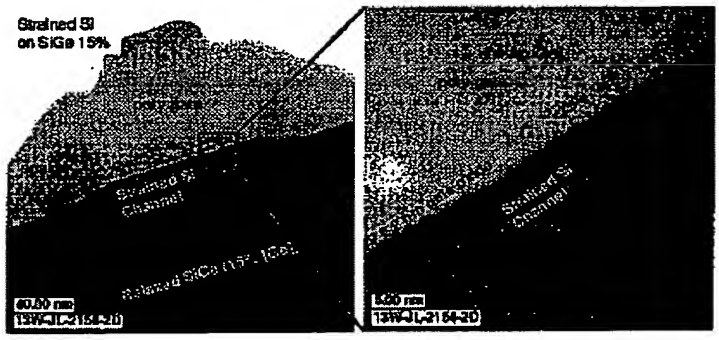
본 양식에는 직무발명의 각 구성요소에 대한 의미와 올바른 작성예가 도움말로 제공됩니다. 본 양식에 기재되어 있는 순서를 따라 작성하되 각 항목별 작성 방법에 대한 도움말은 물음표 아이콘을 선택 후 한번 클릭하면 노란색 메모 패드에 예시와 함께 자세하게 기재되어 있습니다.

< 직 무 발 명 신 고 서 양 식 - 반 도 체 부 문 >

Method of forming a strained non-planar transistor

(간단 명료하되, 발명의 기술분야(장치, 구조, 방법 또는 조성)가 명확히 드러나도록 기재할 것)

Strained Si MOSFET은 향후 scaled device 공정개발에 있어 매우 각광받는 소자구조중 하나이다. 아래 Fig.1에 나타난 바와 같이 lattice mismatch된 layer(예, SiGe)를 channel 하부에 삽입한 구조에서는 기존구조대비 70%이상의 높은 mobility 개선을 나타내고 있다. 이는 통상적인 소자개선 기법으로는 도저히 이루기 힘든 매우 효과적인 성능향상 기법으로서 많은 논문에서 소개되고 있는 실정이다. 하지만, 아직까지 소개된 바로는 Fig.1과 같은 planar MOSFET 구조에서만 보고되고 있고 다른 advanced MOSFET에의 적용은 연구되고 있지 않다.



(A)

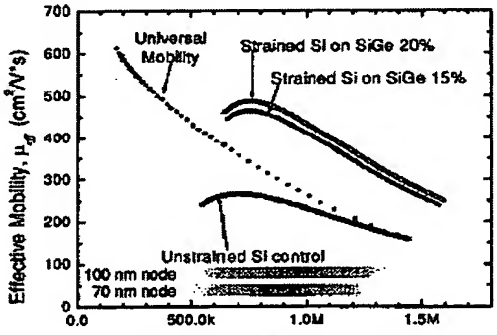


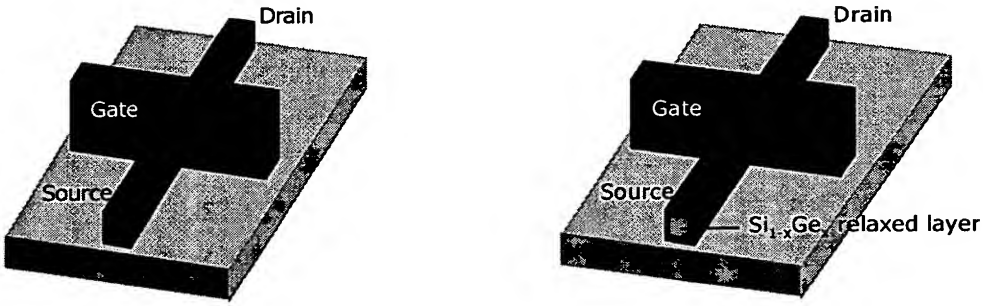
Fig. 8. Effective mobility is enhanced by >70% over the control and universal mobility even at a very high vertical field of >1.0 MV/cm.

(B)

Fig.1 Strained Silicon MOSFET
(A) SEM cross section image (B) measured mobility

본 발명은 65nm 세대이후에 적용되리라 예상되는 multi-gate non-planar구조 소자에 적용한 strained MOSFET에 대한 구조 및 공정특허로서 strained channel이 strain-inducing layer을 감싸는 형태를 특징으로 하고 있다(Fig.2).

Fig.2에서는 double/tri-gate구조의 MOSFET을 도시하였으며, Fig.2(A)와 (B)의 차이를 보면 active bar에 SiGe layer가 삽입된 형태로서 Top과 양쪽 side에 strained channel을 형성한 구조를 보여주고 있다.



(A) (B)

Fig.2 Non-planar MOSFET structure
(A) Conventional (B) Proposed new structure

Abstract (발명의 요약)

(발명이 속하는 기술분야, 발명의 목적, 구성, 효과 등을 간략하게 기술할 것)

본 발명은 향후 sub-65nm세대에 주류를 이루게 될 non-planar MOSFET소자에 대해서 strain-inducing layer가 삽입된 구조를 제안하며, 이로서 70%이상의 mobility 개선기법을 지속적으로 적용할 수 있도록 한다. 기본적인 형성방법은 substrate위에 형성된 strain-inducing layer/Si의 적층구조에서 active define이후에 Si-epi를 성장시켜 active상부와 좌우측면에 Si channel layer가 감싸도록 한다.

Related Arts & Objects of the Invention(종래기술의 문제점 및 그것을 해결하고자 하는 본 발명의 목적)

종래기술에서는 Fig.1과 같이 통상적인 planar MOSFET구조에서 Si-channel 하단부에 SiGe같은 layer을 삽입하여 strained channel을 형성해왔다. 하지만, device가 scaling되어 sub-65nm세대로 진입하면 기존의 planar MOSFET은 더 이상 역할을 하지 못하고 새로운 소자의 출현이 필요하다. 현재까지의 기술동향을 볼때 double/tri-gate 구조가 가장 유력시 되고있으며, 위의 strained-Si 기술을 구현한 예는 아직 존재하지 않았다. 본 발명은 strained-Si 구조를 non-planar구조인 double/tri-gate TR에서 실현하는 기법과 구조를 제안한다.

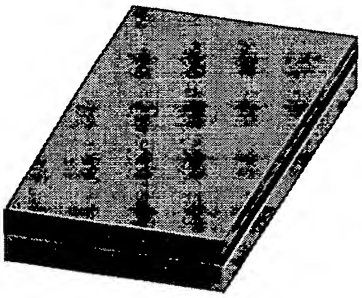
Description of the Invention (발명의 구체적 설명)

Double/Tri-gate MOSFET구조는 이미 많은 논문에서 활발하게 논의되고 있다. 본 발명은 통상적인 double/tri-gate MOSFET process sequence는 그대로 유지하면서 약간의 추가 공정을 도입하는 scheme이다.

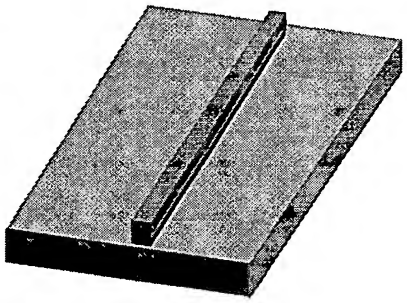
(발명의 실시예)

본 발명의 실시예를 소개하고자 한다. 아래의 일련의 그림들은 process sequency가 진행되는 과정을 도식적으로 나타내고 있으며 그림에서의 color와 pattern은 해당 물질을 표시한다(Legend 참조).

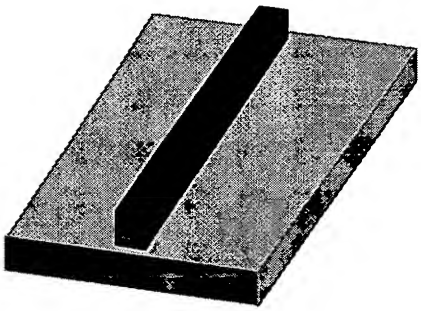
(Fig.3.1)



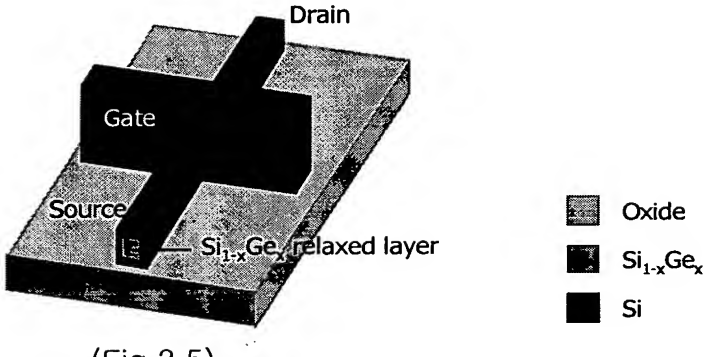
(Fig.3.2)



(Fig.3.3)



(Fig.3.4)



(Fig.3.5)

Fig.3 Process sequence of strained Si double/tri-gate MOSFET

Thin Si layer의 SOI wafer(Fig.3.1)위에 Si과 lattice mismatch 특성을 가지는 물질을 epi로 성장한다. 본 실시예에서는 Si layer의 두께는 10~30nm로 하며, 상기의 Si layer위해 epi성장시키는 물질은 $Si_{1-x}Ge_x$ 을 예로 들며, 성장 두께는 10~90nm를 권장한다(Fig.3.2). 통상적인 active patterning을 진행하여 Fig.3.3의 구조를 형성한후 Si epi를 적당량 진행한다. 이때의 active width는 10nm이상을 통상적인 실시예로 권장하며, Si epi두께는 10~100nm을 권장한다. 다음 과정으로 gate oxide을 형성하고 gate depo & patterning을 진행하여 strained channel을 갖는 double/tri-gate MOSFET을 형성한다.

Proposed Claims or Features of the Invention (청구범위 또는 발명의 특징)

(독립항) Channel의 면방향이 W/F평면과 수직인 성분을 갖는 MOSFET구조에서 Si과 lattice mismatch특성을 갖는 strain-inducing layer가 active내에 삽입되어 있는 있는 소자구조.

(종속항) 상기 독립항의 제조방법은 다음과 같은 일련의 공정으로 이루어진다.

- SOI 기판위에 Si과 lattice mismatch특성의 막(막질1)을 epi로 형성한다.
- 상기의 막질1위에 photo- 또는 hardmask를 적용하여 active를 define한다. 이때의 define된 active는 oxide위에 mesa구조로서 존재한다.
- 상기의 define된 active에 Si epi를 진행하여 상기의 active의 상부와 측면을 Si이 감싸는 구조를 형성한다.
- 통상적인 gate oxide공정을 진행하고 gate물질을 depo하고 photo- 또는 hardmask를 사용하여 gate patterning을 진행한다.
- 통상적인 spacer 형성용 dielectric 막질을 depo & etch하여 spacer를 형성한다.
- Refractory metal(Co, Ni, Pd, Hf)을 depo하고 열처리를 진행하여 metal-silicide을 형성한다.

(종속항) 상기의 종속항에서 필요한 경우에는 공정 과정중에 불순물 이온주입을 진행할 수 있고 상기의 일련의 공정의 앞과 뒤에 추가적인 공정을 진행할 수 있다.

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Serial No. 10/801,651	:	Examiner Walter L. Lindsay Jr.
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SEMICONDUCTOR DEVICE WITH DIFFERENT LATTICE PROPERTIES

SUMBISSION OF ENGLISH-LANGUAGE TRANSLATION

U.S. Patent and Trademark Office
Customer Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Attached is a true and accurate English-language translation of the DISCLOSURE OF EMPLOYEE'S INVENTION appended to the YANG DECLARATION having an execution date of March 28, 2006.

Respectfully submitted,

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April 10, 2006

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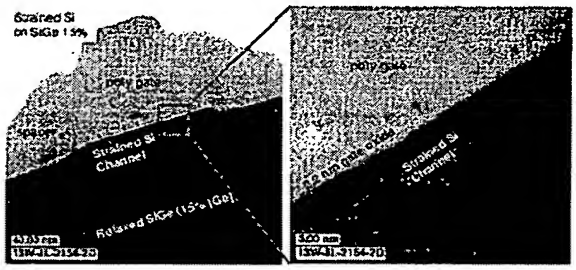
<DISCLOSURE OF EMPLOYEE'S INVENTION - SEMICONDUCTOR DEPARTMENT>

Method of forming a strained non-planar transistor

A strained-Si metal-oxide semiconductor field-effect transistor (MOSFET) is one of the much-spotlighted devices in a development of processing a scaled–down device. As shown in the following FIG. 1, the strained-Si MOSFET shows 70% more improved mobility than that of a conventional structure, in which a lattice-mismatched layer (for example, an SiGe layer) is inserted under a channel. This structure is a remarkably effective for improving performance, and it is difficult for the conventional structure to achieve this effect. This structure has been published in many papers. However, this structure has thus far only been applied to a planar MOSFET structure as shown in FIG. 1. Applications to other advanced MOSFETs have not been studied yet.



(A)

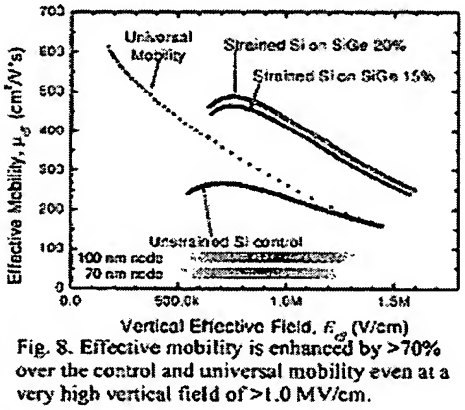


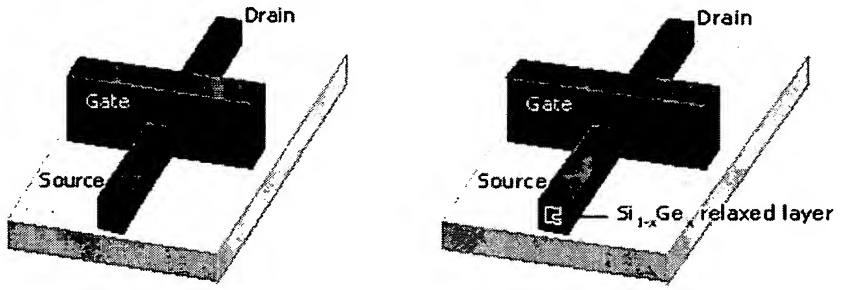
Fig. 8. Effective mobility is enhanced by >70% over the control and universal mobility even at a very high vertical field of >1.0 MV/cm.

(B)

Fig. 1 Strained-Silicon MOSFET

(A) SEM cross section image (B) Measured mobility

The present invention provides a strained MOSFET structure and a method of forming the same that can be applied to a multi-gate and non-planar structure having a line width of below about 65nm. The feature of the present invention is that a strained channel surrounds a strain-inducing layer (FIG. 2).



(A) (B)

Fig. 2 Non-planar MOSFET structure

(A) Conventional (B) Proposed new structure

FIG. 2 illustrates a MOSFET device having a double/triple gate structure. Comparing FIG. 2(B) with FIG. 2(A), an SiGe layer is inserted within an active bar, and a strained channel is formed on a top side and both sides of the active bar in FIG. 2(B).

Abstract

The present invention provides a non-planar metal-oxide semiconductor field-effect transistor (MOSFET) device including a strain-inducing layer and a method of forming the same, which is mainly used in a sub-65nm generation device manufacturing. According to the present invention, mobility is improved by more than about 70%. In the method, a strain-inducing layer and an Si layer are formed on a substrate. An active region is defined. An Si-epitaxial layer is formed, and thus an Si channel layer surrounds a top side, a right side and a left side of the active region.

Related Arts & Objects of the Invention

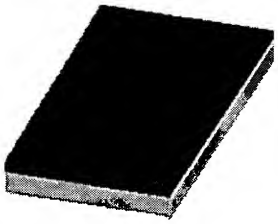
In a conventional method, a strained channel is formed by inserting an SiGe layer into a bottom of an Si-channel in a general planar metal-oxide semiconductor field-effect transistor (MOSFET) structure as shown in FIG. 1. However, as a device is scaled down, a conventional planar MOSFET cannot perform a role in a device having a design rule of below about 65nm, and thus a device having a novel structure is needed. In view of technology trends thus far, a double/triple gate structure is becoming a leading structure type, and examples embodying the above-mentioned strained-Si structure has not yet been disclosed. The present invention provides a device embodying a strained-Si structure in a non-planar double/triple gate, and a method of forming the same.

Description of the Invention

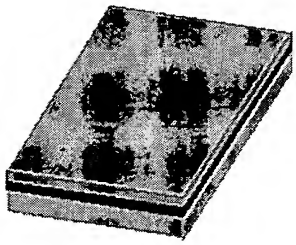
A double/triple gate metal-oxide semiconductor field-effect transistor (MOSFET) structure has been already discussed in many papers. According to the present invention, an additional process is employed to a conventional method of forming a double/triple gate MOSFET structure.

(Example embodiment of the present invention)

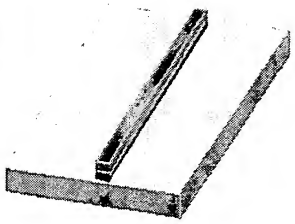
An example embodiment of the present invention will be described. A series of the following pictures illustrates a process of the present invention. Colors and patterns in figures represent corresponding materials (see legend).



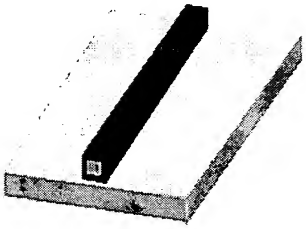
(Fig. 3.1)



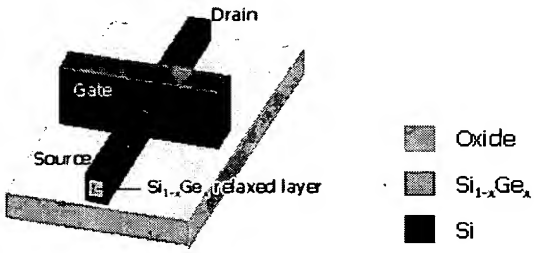
(Fig. 3.2)



(Fig. 3.3)



(Fig. 3.4)



(Fig. 3.5)

Fig. 3 Process sequence of strained-Si double/tri-gate MOSFET

A thin Si layer is formed on a silicon-on-insulator (SOI) wafer (FIG. 3.1). A material having a lattice mismatch with respect to Si is epitaxially grown on the thin Si layer. In the present embodiment, a thickness of the thin Si layer is about 10nm to about 30nm. An example of the material that is epitaxially grown on the thin Si layer is $Si_{1-x}Ge_x$, and a thickness of an $Si_{1-x}Ge_x$ layer is about 10nm to about 90nm (FIG. 3.2). A normal patterning process is performed on the Si layer and the $Si_{1-x}Ge_x$ layer to form a structure as shown in FIG. 3.3, and Si is epitaxially grown. Then, a width of an active region is more than about 10nm and a thickness of an Si epitaxial layer is about 10nm to about 100nm. Next, a gate oxide layer and a gate electrode are formed and patterned to form a double/triple gate MOSFET having a strained channel.

Proposed Claims or Features of the Invention

1. A metal-oxide semiconductor field-effect transistor (MOSFET) device of which a face direction of a channel is perpendicular to a W/F plane, wherein a strain-inducing layer having a lattice mismatch with respect to Si is inserted within an active region.

2. A method of forming a MOSFET device comprising:

forming a layer on a silicon-on-insulator (SOI) substrate by epitaxially growing a material having a lattice mismatch with respect to silicon;

defining an active region by using a first photoresist pattern or a first hard mask, wherein the active region has a mesa structure;

epitaxially growing silicon on the active region to form a structure in which silicon surrounds a top side and both sides of the active region;

forming a gate oxide layer and a gate electrode, and patterning the gate oxide layer and the gate electrode using a second photoresist pattern or a second hard mask;

forming a spacer by depositing and etching a dielectric material; and

forming a metal-silicide layer by depositing and heat-treating a refractory metal selected from the group consisting of Co, Ni, Pd and Hf.

3. The method of claim 2, further comprising performing an ion implantation process, and further comprising performing an additional process, before forming the layer on the SOI substrate or after forming the metal-silicide layer.